Course No.	Course Name	L-T-P -Credits	Year of Introduction
EE204	Digital Electronics and Logic Design	2-1-0-3	2016

Prerequisite : Nil

Course Objectives

To impart knowledge about digital logic and to gain the ability to design various digital circuits

Syllabus

Review of Number Systems and Codes, Digital Logic, Combinational Logic Circuits, Data Processing Circuits, Arithmetic Circuits, Flip-Flops, Registers, Counters, DACs and ADCs, Design of synchronous Sequential Circuits, Introduction to HDL.

Expected outcome.

After the successful completion of the course, the student will be able to:

1. Familiar with various number systems and Boolean algebra
2. design and analyse any digital logic gate circuits and Flip flop based systems.
3. Familiar with combinational circuits
4. gain the capability of implementing various counters,
5. describe the operation of ADC and DAC circuits
6. acquire basic knowledge on VHDL

Text Book:

1. Floyd T.L, Digital Fundamentals , 10/e, Pearson Education, 2011

2. C.H.Roth and L.L.Kimney Fundamentals of Logic Design, 7/e, Cengage Learning, 2013

References:

1. Donald P Leach, Albert Paul Malvino and GoutamSaha., Digital Principles and Applications, 8/e, by Mc Graw Hill
2. Mano M.M, Logic and Computer Design Fundamentals, 4/e, , Pearson Education.
3. Tocci R.J and N.S.Widmer, Digital Systems, Principles and Applications, 11/e, , Pearson Education.
4. John F. Wakerly, Digital Design: Principles and Practices, 4/e, , Pearson, 2005
5. Taub & Schilling: Digital Integrated Electronics, McGraw Hill,1997

Data Book (Approved for use in the examination):Nil

Course Plan			
Module	**Contents**	**Hours**	**Sem.ExamMarks**
I	Number Systems and Codes : Binary, Octal and hexadecimal conversions- ASCII code, Excess -3 code, Gray code, Error detection and correction - Parity generators and checkers – Fixed point and floating point arithmetic. Binary addition and subtraction, unsigned and signed numbers, 1's complement and 2's complement arithmetic.	**7 hours**	15%
II	TTL logic and CMOS logic - Logic gates, Universal gates - Boolean Laws and theorems, Sum of Products method, Product of Sum method – K map representation and simplification(upto four variables) - Pairs, Quads, Octets, Dont care conditions.	**7 hours**	15%
FIRST INTERNAL EXAMINATION			
III	Combinational circuits: Adders _ Full adder and half adder – Subtractors, halfsubtractor and fullsubtractor – Carry Look ahead adders – ALU(block diagram only). Multiplexers, Demultiplexers, Encoders, BCD to decimel decoders.	**7 hours**	15%
IV	Sequential circuits: Flip-Flops, SR, JK, D and T flip-flops, JK Master Slave Flip-flop, Conversion of flip-flops, Registers -SISO,SIPO, PISO, PIPO. Counters : Asynchronous Counters – Modulus of a counter – Mod N counters.	**8 hours**	15%
SECOND INTERNAL EXAMINATION			
V	Synchronous counters: Preset and clear modes, Counter Synthesis: Ring counter, Johnson Counter, Mod N counter, Decade counter. State Machines: State transition diagram, Moore and Mealy Machines – Design equation and circuit diagram.	**7 hours**	20%
VI	Digital to Analog conversion – R-2R ladder, weighted resistors. Analog to Digital Conversion - Flash ADC, Successive approximation, Integrating ADC.	**8 hours**	20%

	Memory Basics, Read and Write, Addressing, ROMs, PROMs and EPROMs, RAMs, Sequential Programmable Logic Devices - PAL, PLA, FPGA (Introduction and basic concepts only) Introduction to VHDL, Implementation of AND, OR, half adder and full adder.		
END SEMESTER EXAM			

QUESTION PAPER PATTERN (End semester exam)

Part A: 8 questions.

One question from each module of Module I - IV; and two each from Module V & VI.

Student has to answer all questions. (8 x5)=40

Part B: 3 questions uniformly covering modules I&II

Student has to answer any 2 questions: (2 x 10) =20

Part C: 3 questions uniformly covering modules III&IV

Student has to answer any 2 questions: (2 x 10) =20

Part D: 3 questions uniformly covering modules V&VI

Student has to answer any 2 questions: (2 x 10) =20

Note: Each question can have maximum of 4 sub questions, if needed.